IN THE CLAIMS:

Please amend the claims as follows:

1. (previously presented) A circuit arrangement, for power semiconductor modules, comprising:

at least one electrically insulating substrate;

at least two mutually insulated ribbon connectors on said substrate;

at least one power semiconductor component attached to at least one of said ribbon connectors;

at least a first and a second DC port conductors and at least one AC port conductor;

said DC port conductors being arranged proximate to each other and at least one of said substrate and said ribbon conductors;

each said DC port conductor including at least a first substantial length portion in parallel to a second respective substantial length portion on said second DC port conductor;

said AC port conductor having at least one portion proximate at least one of said substrate surface and said ribbon connectors;

at least one surface element extending at least at a first angle from one of said AC port conductor and said DC port conductors; and

at least one electrical connection extending from said at least one surface element to at least one of said power semiconductor component and said at least one ribbon conductor, whereby said circuit arrangement provides a low parasitic inductance and a low ohmic resistance in a power semiconductor module.

2. (previously presented) A circuit arrangement, according to claim 1, wherein:

said first angle is a ninety degree angle, whereby said at least one surface element extends substantially parallel to said substrate.

3. (canceled)

4. (previously presented) A circuit arrangement, according to claim 1, wherein:

each said DC port conductor is arranged proximate said ribbon conductors;

said DC port conductors and said at least one surface element being electrically insulated from said ribbon conductors, whereby no direct electrical link exists between said DC port conductors and said ribbon conductor;

said AC port conductors are arranged proximate said ribbon conductor; and

said AC port conductors being electrically insulated from said ribbon conductors, whereby no direct electrical link exists between said AC port conductors and said ribbon conductor.

5. (previously presented) A circuit arrangement, according to claim 1, further comprising:

projecting end portions on each respective said DC and AC port conductors extending away from said substrate; and

each respective projecting portion including at least one respective contact element for securing external electrical contacting of said power semiconductor module to said port conductor.

6. (previously presented) A circuit arrangement according to claim 5, further comprising:

a housing bounding said power semiconductor module and said circuit;

said housing enclosing said at least one substrate and mechanically supporting respective said DC and AC port conductors;

said housing including at least two spaced apart recesses; and

said projecting end portions extending through said spaced apart recesses enabling simple electrical connection thereto while said housing provides electrical protection to said circuit.

7. (previously presented) A circuit arrangement according to Claim 1, wherein:

said at least one electrical connection is a wire bond connection, whereby said wire bond connection and said at least one surface element enable simple electrical connection during an assembly of said circuit while maintaining low parasitic induction of said circuit.

8. (previously presented) A circuit arrangement according to Claim 1, further comprising:

at least one sensor component on at least one of said substrate and said at least one ribbon connector.

9. (previously presented) A circuit arrangement according to Claim 1, further comprising:

at least one recess defined in at least one of said DC and said AC port conductors; and

said at least one recess is on a side of said at least one port conductor facing said at least one substrate, whereby a base of said recess is further from said at substrate than a bottom surface of said at least one port conductor.

10. (currently amended) A circuit arrangement according to Claim 1, further comprising:

at least one electrical insulation layer; and

said at least one insulation layer extending between at least a portion of one of said DC port ~~conductor~~ conductors and at least one of said at least two [[one]] ribbon ~~connector~~ connectors.

11. (previously presented) A circuit arrangement according to Claim 10, further comprising:

an extension layer of said electrical insulating layer extending between said at least one surface element and one of said ribbon connector and said substrate.

12. (previously presented) A circuit arrangement according to Claim 1, further comprising:

at least one base element extending from a bottom surface of at least one of said DC and said AC port conductors; and

said at least one base element supporting said at least one port conductor on said at least one substrate.

13. (previously presented) A circuit arrangement, according to claim 1, further comprising:

at least one metal lamination on said substrate opposite on an opposite side of said substrate from said at least one ribbon connector.

14. (previously presented) A circuit arrangement, according to claim 1, further comprising:

at least one electrical insulation layer;

said at least one insulation layer extending between at least a portion of one of said DC port conductor and said at least one ribbon connector;

an extension layer of said electrical insulating layer extending between said at least one surface element and one of said ribbon connector and said substrate;

at least one base element extending from a bottom surface of at least one of said DC and said AC port conductors; and

said at least one base element supporting said at least one port conductor on said at least one substrate.

15. (previously presented) A circuit arrangement, for power semiconductor modules, comprising:

at least one electrically insulating substrate;

at least two mutually insulated ribbon connectors on said substrate;

at least one power semiconductor component attached to at least one of said ribbon connectors;

at least a first and a second DC port conductors and at least one AC port conductor;

said DC port conductors being arranged proximate to each other and at least one of said substrate and said ribbon conductors;

each said DC port conductor including at least a first substantial length portion in parallel to a second respective substantial length portion on said second DC port conductor;

said AC port conductor having at least one portion proximate at least one of said substrate surface and said ribbon connectors;

at least one surface element extending at least at a first angle from one of said AC port conductor and said DC port conductors;

at least one electrical connection extending from said at least one surface element to at least one of said power semiconductor component and said at least one ribbon conductor;

at least one electrical insulation layer; and

said at least one insulation layer extending between at least a portion of one of said DC port conductor and said at least one ribbon connector, whereby said circuit arrangement provides a low parasitic inductance and a low ohmic resistance in a power semiconductor module.

16. (previously presented) A circuit arrangement according to Claim 15, further comprising:

an extension layer of said electrical insulating layer extending between said at least one surface element and one of said ribbon connector and said substrate.

17. (previously presented) A circuit arrangement according to Claim 16, further comprising:

at least one base element extending from a bottom surface of at least one of said DC and said AC port conductors; and

said at least one base element supporting said at least one port conductor on said at least one substrate.

18. (previously presented) An electrical device, comprising:

a power semiconductor module;

said power semiconductor module including a circuit arrangement comprising:

at least one electrically insulating substrate;

at least two mutually insulated ribbon connectors on said substrate;

at least one power semiconductor component attached to at least one of said ribbon connectors;

at least a first and a second DC port conductors and at least one AC port conductor;

said DC port conductors being arranged proximate to each other and at least one of said substrate and said ribbon conductors;

each said DC port conductor including at least a first substantial length portion in parallel to a second respective substantial length portion on said second DC port conductor;

said AC port conductor having at least one portion proximate at least one of said substrate surface and said ribbon connectors;

at least one surface element extending at least at a first angle from one of said AC port conductor and said DC port conductors;

at least one electrical connection extending from said at least one surface element to at least one of said power semiconductor component and said at least one ribbon conductor;

at least one electrical insulation layer; and

said at least one insulation layer extending between at least a portion of one of said DC port conductor and said at least one ribbon connector, whereby said circuit arrangement provides a low parasitic inductance and a low ohmic resistance in a power semiconductor module.

19. (previously presented) A circuit arrangement according to Claim 18, further comprising:

an extension layer of said electrical insulating layer extending between said at least one surface element and one of said ribbon connector and said substrate.

20. (previously presented) A circuit arrangement according to Claim 19, further comprising:

at least one base element extending from a bottom surface of at least one of said DC and said AC port conductors; and

said at least one base element supporting said at least one port conductor on said at least one substrate.

21. (previously presented) A circuit arrangement, with low inductances and low ohmic resistance in the current inputs and outputs in a power semiconductor modules, comprising:

at least one electrically insulating substrate;

a plurality of mutually insulated metallic ribbon connectors applied to said substrate;

at least one power semiconductor component attached to at least one of respective said ribbon connectors;

at least a first and a second DC port conductors and at least one AC port conductor;

said DC port conductors being arranged proximate to each other and at least one of said substrate and said ribbon conductors;

each said DC port conductor including at least a substantial length portion in parallel to a second respective substantial length portion on said second DC port conductor;

at least one AC port conductor having at least one portion in close proximity to one of said substrate surface and said ribbon connectors;

at least one of said DC port conductors and said AC port conductor include at least one surface element ;

said at least one surface element extending substantially parallel to a surface of said substrate; and

at least one electrical connection extending from said at least one surface element to at least one of said power semiconductor component and said at least one ribbon conductor, whereby said circuit arrangement provides a low parasitic inductance in a power semiconductor module.

22. (previously presented) A circuit arrangement, according to claim 21, wherein:

said DC port conductors are arranged proximate said ribbon conductors;

said DC port conductors being electrically insulated from said ribbon conductors, whereby no direct electrical link exists between said DC port conductors and said ribbon conductor;

said AC port conductors are arranged proximate said ribbon conductor; and

said AC port conductors being electrically insulated from said ribbon conductors, whereby no direct electrical link exists between said AC port conductors and said ribbon conductor.

23. (previously presented) A circuit arrangement according to Claim 21, wherein:

said power semiconductor module is provided with a housing that encloses said at least one substrate and supports respective said DC and AC port conductors mechanically;

said housing including at least two spaced apart recesses;

extending portions of respective said DC and AC port conductors extending through said recesses away from said housing; and

each respective said extending portion including a respective contact element for securing external electrical contacting of said power semiconductor module.

24. (previously presented) A circuit arrangement according to Claim 21, wherein:

said at least one electrical connection is a wire bond connection.

25. (previously presented) A circuit arrangement according to Claim 21, further comprising:

at least one sensor component arranged on at least one of said substrate and said at least one ribbon connector.

26. (previously presented) A circuit arrangement according to Claim 21, wherein:

at least one of said DC and said AC port conductors includes at least one recess; and

said at least one recess is on a side of said at least one port conductor facing said at least one substrate.

27. (currently amended) A circuit arrangement according to Claim 21, further comprising:

an electrical insulation layer between at least a portion of at least one of said at least [[one]] two DC port ~~conductor~~ conductors and said at least one ribbon connector.

28. (previously presented) A circuit arrangement according to Claim 27, wherein:

said electrical insulating layer extends below said at least one surface element.

29. (previously presented) A circuit arrangement according to Claim 21, wherein:

at least one base element is on at least one of said DC and said AC port conductors, whereby said at least one base element supports said at least one port conductor relative to said at least one substrate.